

TECHNICAL MANUAL

**ORGANIZATIONAL MAINTENANCE MANUAL
RADAR INTERFACE EQUIPMENT MAINTENANCE**

**16K MEMORY
VIDEO SIMULATOR UNIT**

**EXPANDED TROUBLESHOOTING
LOGIC DIAGRAMS**

**GUIDED MISSILE AIR DEFENSE SYSTEM
AN/TSQ-73**

**HEADQUARTERS, DEPARTMENT OF THE ARMY
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ORGANIZATIONAL MAINTENANCE MANUAL
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16K MEMORY, VIDEO SIMULATOR UNIT

EXPANDED TROUBLESHOOTING
(LOGIC DIAGRAMS)

GUIDED MISSILE AIR DEFENSE SYSTEM
AN/TSQ-73

REPORTING OF ERRORS

You can help improve this publication. If you find any mistakes, or if you know of a way to improve the procedures, please let us know. Mail your letter or DA Form 2028-2, located in back of this manual direct to: Commander, U.S. Army Missile Command, ATTN: AMSMI-MMC-LE-A-P, Redstone Arsenal, AL 35898-5238. A reply will be furnished to you.

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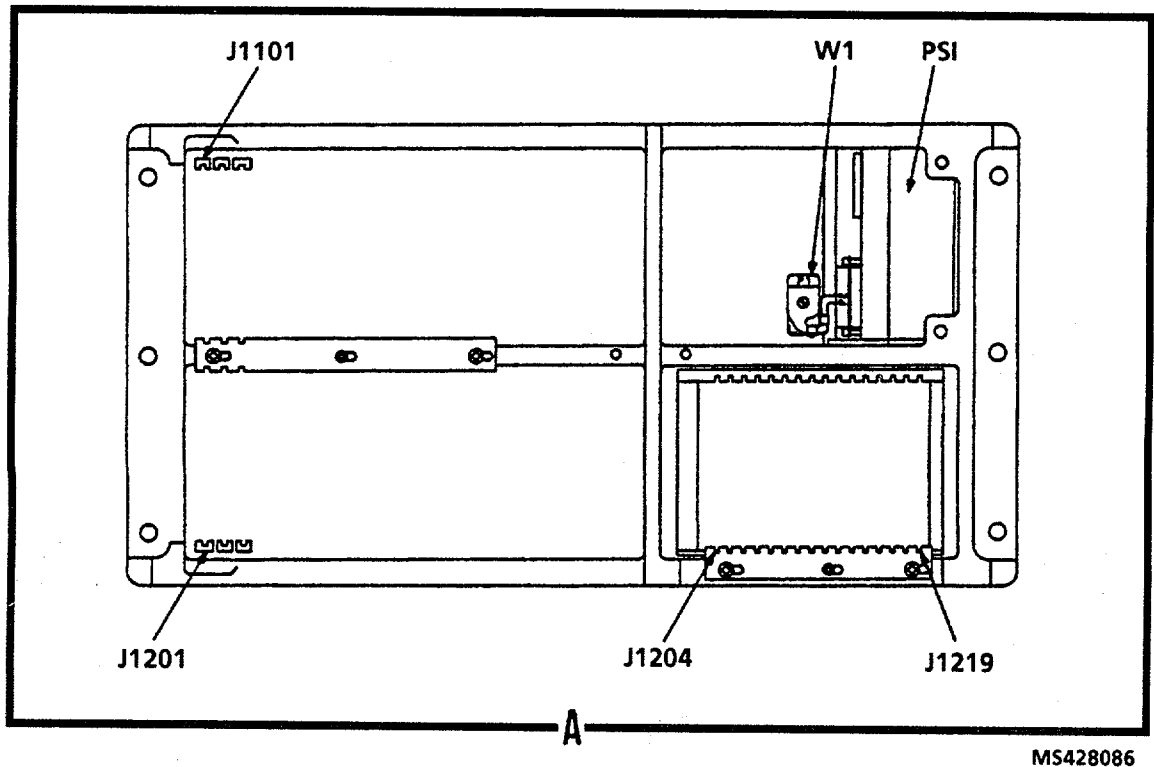
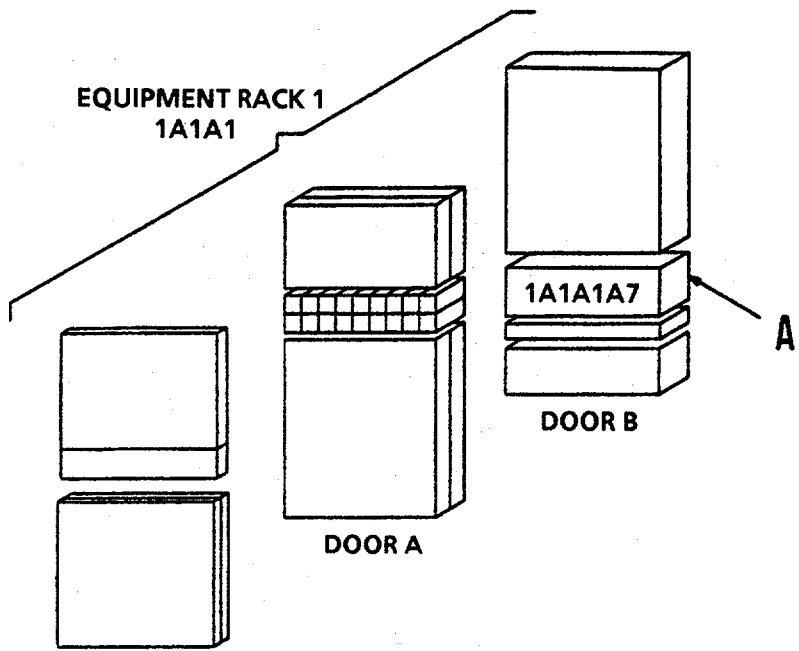
Section XVI. 16K MEMORY AND VIDEO SIMULATOR UNIT

5-51. General. This manual is Volume 6 of TM 9-1430-655-20-3, Radar Interface Equipment Maintenance for Guided Missile Air Defense System AN/TSQ-73. It contains the logic diagrams covering the single port 16K Memory and Video Simulator Unit for the use and guidance of advanced personnel responsible for repair of the RIE. Foldout 206 covers the 16K memory and foldouts 207 through 260 cover the VSU. The single port 16K memory unit is located in the center section of rack 1, 1A1A1, door B. The VSU is a single bay of circuit cards mounted in the front door of the lower rear section of rack 1, 1A1A1. Figure 5-6 illustrates the location of the 16K memory units and figure 5-7 illustrates the location of the VSU.

5-52. Logic Diagram. Logic diagrams provide the maintenance technician pin to pin signal flow, traceable by signal mnemonics, and I/O tables, to help identify faulty cards and to troubleshoot faults in the backplane

wiring and other areas that are beyond fault isolation capabilities of the MTS.

5-53. Using Logic Diagrams. The logic diagrams for the 16K memory provide circuit card pin to pin signal flow traceable within foldouts by signal mnemonics and between foldouts by signal mnemonics and alpha connectors. Table 5-40.1 contains the circuit card slot and the part number of the card. Signal flow for the VSU is traceable between circuit card pin numbers and is shown as inputs and outputs of integrated circuit logic devices on the circuit card. A specific signal can be followed between foldouts by using the signal mnemonic and the logic diagram input/output table. The circuit card slot is shown within the integrated circuit card device symbol. Table 5-41 contains the circuit slot and the part number of the card. Table 5-42 contains, by card part number, the test point for each of the 80 pins of MTS testable cards in the VSU.



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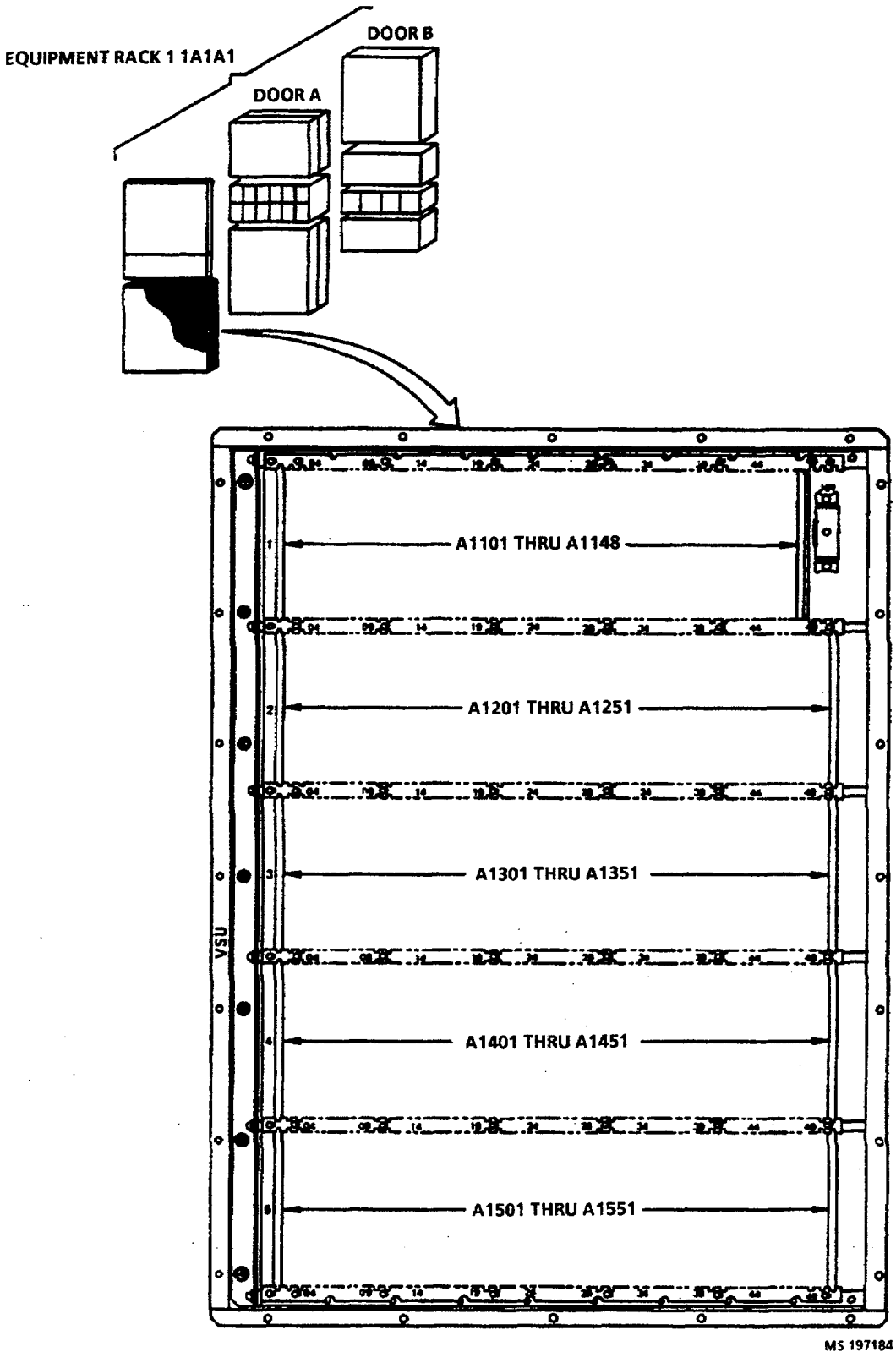
Figure 5-6. Single-Port 16K Memory Unit 1A1A1A7, Component Location

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Table 5-40.1. Single-Port 16K Memory Unit 1A1A1A7, Circuit Card Location

Card slot	Part number	Card type	Color code			
			1	2	3	4
SHELF 1						
A1101	W386	Connector	-	-	-	-
A1101	W387	Connector	-	-	-	-
A1103	W540	Connector	-	-	-	-
SHELF 2						
A1201	W406	Connector	-	-	-	-
A1202	W407	Connector	-	-	-	-
A1203	W541	Connector	-	-	-	-
A1204	-	-	-	-	-	-
A1205	13143778	Timing and Control	-	-	-	-
A1206	13143777	CMOS Storage	-	-	Orange ¹	
A1207	13143777	CMOS Storage	-	-	Orange ¹	
A1208	13143777	CMOS Storage	-	-	Orange ¹	
A1209	13143777	CMOS Storage	-	-	Orange ¹	
A1210	13143777	CMOS Storage	-	-	Orange ¹	
A1211	13143777	CMOS Storage	-	-	Orange ¹	
A1212	13143777	CMOS Storage	-	-	Orange ¹	
A1213	13143777	CMOS Storage	-	-	Orange ¹	
A1214	13143777	CMOS Storage	-	-	Orange ¹	
A1215	13143777	CMOS Storage	-	-	Orange ¹	
A1216	13143777	CMOS Storage	-	-	Orange ¹	
A1217	10283626	Quad NAND gate	Orange	Blue	Red	Blue
A1218	-	-	-	-	-	-
A1219	-	-	-	-	-	-

¹13143777 cards have orange edge to identify CMOS devices; these cards are not testable by MTS and require special handling. Refer to CMOS cautionary notice on page a of this technical manual.



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Figure 5-7. Video Simulator Unit 1A1A1A3, Component Location.

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