

TECHNICAL MANUAL

**ORGANIZATIONAL MAINTENANCE MANUAL
RADAR INTERFACE EQUIPMENT MAINTENANCE
VIDEO PROCESSOR UNIT 1 AND 2**

**EXPANDED TROUBLESHOOTING
(LOGIC DIAGRAMS)**

**GUIDED MISSILE
AIR DEFENSE SYSTEM
AN/TSQ-73**

Change
No. 9-1430-655-20-3-4



HEADQUARTERS
DEPARTMENT OF THE ARMY
Washington, D.C., 21 January 1985

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REPORTING OF ERRORS

You can help improve this publication. If you find any mistakes, or if you know of a way to improve the procedures, please let us know. Mail your letter, DA Form 2028 (Recommended Changes to Publications and Blank Forms), or DA Form 2028-2 located in back of this manual direct to: Commander, U.S. Army Missile Command, ATTN: AMSMI-LCME-P, Redstone Arsenal, AL 35898-5238. A reply will be furnished to you.

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Section XIV. VIDEO PROCESSOR UNITS

5-45. General. This manual is Volume 4 of TM 9-1430-655-20-3, Radar Interface Equipment Maintenance for Guided Missile Air Defense System AN/TSQ-73. It contains the logic diagrams covering video processor units (VPU) 1 and 2 for use and guidance of advanced personnel responsible for repair of the RIE. Foldouts 1 through 59 cover VPU 1 and foldouts 60 through 125 cover VPU 2. VPU 1 and 2 are located in equipment rack 1, 1A1A1, door A, in two card cage bays. Figure 5-2 illustrates bay 1 and figure 5-3 illustrates bay 2.

5-46. Logic Diagram. The logic diagrams in this manual provide the maintenance technician pin to pin signal flow, traceable by signal mnemonics and I/O tables, to help identify faulty cards and to troubleshoot faults in the backplane wiring and other areas that are beyond fault isolation capabilities of the MTS.

5-47. Using Logic Diagrams. Logic diagrams in this manual show signal flow in functional subsystems of VPU 1 and 2. Signal flow is traceable between circuit card pin numbers and is shown as inputs and outputs of integrated circuit logic devices on the circuit card. A specific signal can be followed between foldouts by using the signal mnemonic and the logic diagram input/output table. The circuit card slot is shown within the integrated circuit card device symbol. Table 5-37 contains the circuit card slot and the part number of the card. Table 5-38 contains, by card part number, the test point for each of the 80 pins of MTS testable cards.

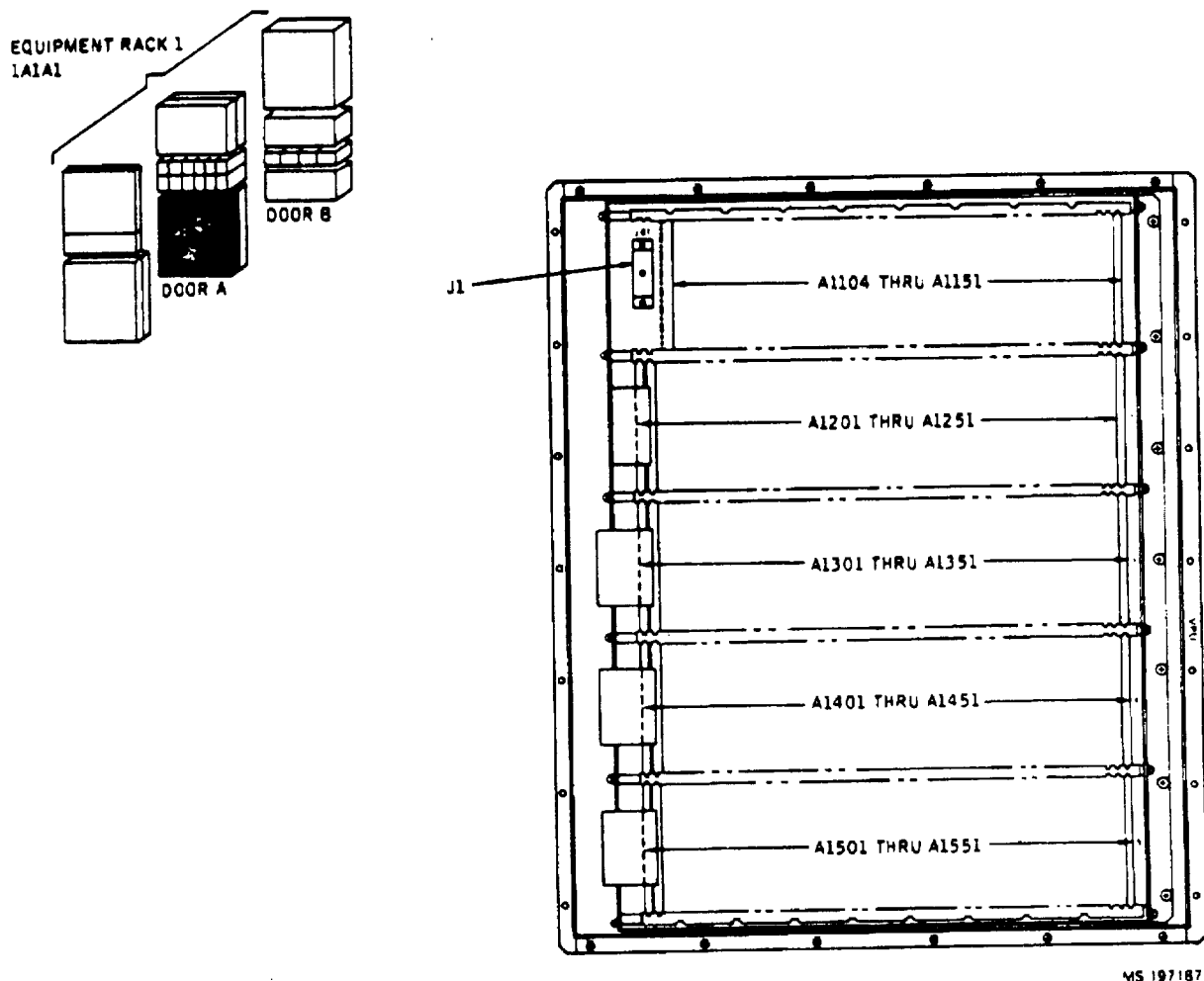
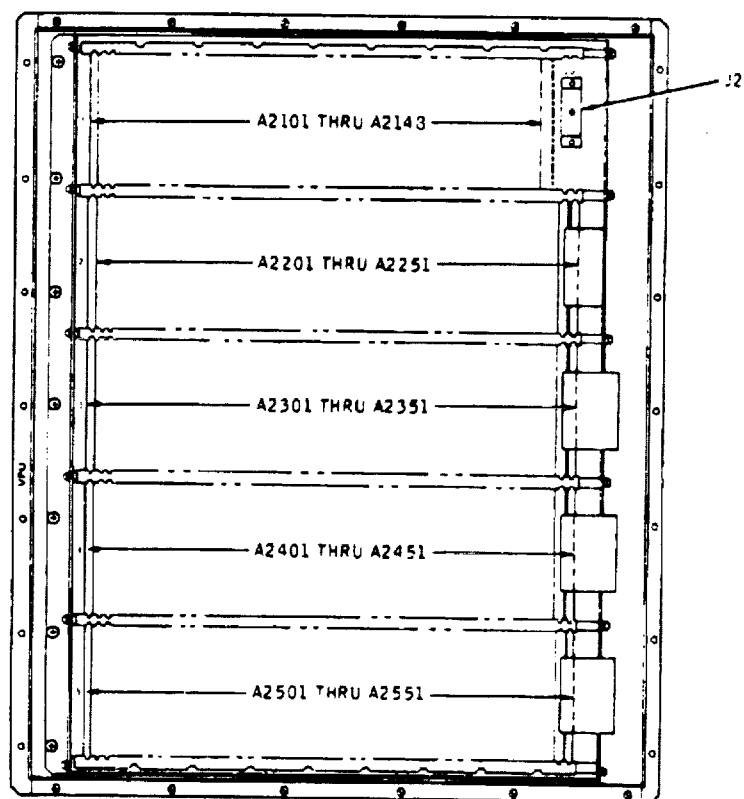
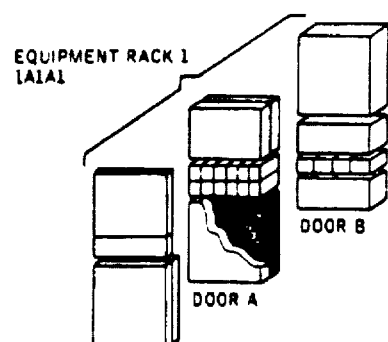


Figure 5-2. Video Processor Unit 1A1A1S Bay 1, Component Location
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Figure 5-3. Video Processor Unit 1A1A1A5 Bay 2, Component Location

5-756 Change 1

Table 5-37. Video Processor Unit 1A1A1A5, Circuit Card Location

CARD SLOT	PART NUMBER	CARD TYPE	COLOR CODE			
			1	2	3	4
BAY-SHELF 1						
A1101	-	-	-	-	-	-
A1102	-	-	-	-	-	-
A1103	-	-	-	-	-	-
A1104	W390	Connector	-	-	-	-
A1105	W391	Connector	-	-	-	-
A1106	W532	Connector	-	-	-	-
A1107	10281606	Hex 4-bit shift register	Brown	Blue	Black	Blue
A1108	10281606	Hex 4-bit shift register	Brown	Blue	Black	Blue
A1109	10281606	Hex 4-bit shift register	Brown	Blue	Black	Blue
A1110	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1111	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1112	-	-	-	-	-	-
A1113	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A1114	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1115	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A1116	587117-102	Hex inverter	Brown	-	Violet	-
A1117	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1118	587108-102	Single 8-input NAND gate	-	-	Gray	-
A1119	-	-	-	-	-	-
A1120	10281652	3-input J-K flip-flop	Brown	Blue	Green	Red
A1121	10281652	3-input J-K flip-flop	Brown	Blue	Green	Red
A1122	10281652	3-input J-K flip-flop	Brown	Blue	Green	Red
A1123	10281603	4-bit multiplexer	Brown	Blue	Black	Orange
A1124	10281603	4-bit multiplexer	Brown	Blue	Black	Orange
A1125	10281602	Counter/decoder	Brown	Blue	Black	Red
AI 126	10281602	Counter/decoder	Brown	Blue	Black	Red
A1127	10281602	Counter/decoder	Brown	Blue	Black	Red
A1128	10281606	Hex 4-bit shift register	Brown	Blue	Black	Blue
A1129	10281606	Hex 4-bit shift register	Brown	Blue	Black	Blue
A1130	-	-	-	-	-	-
A1131	-	-	-	-	-	-
A1132	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A1133	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A1134	587104-102	Dual 4-input NAND gate	-	-	Yellow	-